REMARKS

Claims 1, 3 to 11, 13 and 20 to 24 are pending in this application, of which claims 1, 6 and 9 are the independent claims. Favorable reconsideration and further examination are respectfully requested.

Applicant acknowledge the Examiner's indication that claims 4 and 8 would be allowable if rewritten to overcome the objections and in independent form to include the base claim and any intervening claims; however, Applicant believes he is entitled to broader claims.

Initially, the Examiner objected to informalities in the claims. Specifically, the Examiner objected to the use of "common source" gain stage in claims 1 to 4, 11 and 13 as being allegedly incorrect. Applicant has amended the claims to more distinctly claim the invention. At the Examiner's suggestion, Applicant has inserted the word "the" after "wherein" in claim 8 and deleted the word "and" and added a comma after "11" in claim 13. Applicants have also amended claim 11 to correct the antecedent basis for "the output node". Applicant respectfully request withdrawal of the claims objections.

Turning to the art rejections, claims 1 to 3, 5 to 7, 9 to 11 and 13 were rejected under 35 U.S.C. § 102(e) as being anticipated by Kona et al. (U.S. Patent No. 6,850,049) and under U.S.C. § 103(a) as being obvious over Jaussi et al. (U.S. Patent No. 6,737,909) and obvious over Narendra et al. (U.S. Patent No. 6,448,811).

Claim 1, as amended, is directed to a current compensation circuit. The compensation current includes an impedance divider directly coupled to a supply voltage source of a current

mirror circuit and having an output node. The impedance divider is configured to generate a compensation signal at the output node representative of voltage changes in the supply voltage source. The compensation current also includes a gain stage having a stage input coupled to the output node and a stage output connected to a node of the current mirror circuit. The gain stage is configured to generate a compensation current from the stage output for application to the node of the current mirror circuit in response to the compensation signal. The gain stage is directly coupled to the supply voltage source and includes a first parallel array of programmable transistors for defining a predetermined range of the compensation current.

The applied art is not understood to disclose or suggest the foregoing features of claim 1.

With respect to the §102 rejection, Kono does not disclose or suggest a gain stage being directly coupled to the supply voltage source.

In particular, the Examiner has indicated that a "common-drain gain stage" is "the combination of Field Effect Transistors (FETs) between the current mirror and ground" (see page 3 of the Office Action), which Applicant understands are FETs MN12 and MN13. FETs MN12 and MN13 are not directly connected to the supply voltage. Furthermore, FETs MN12 and MN13 form a current mirror not a gain stage (see column 9, lines 1 to 3 of Kono). Moreover, the Examiner has indicated that the impedance divider includes a resistor (RLO) and FETs MP13 and MN13 (see page 3 of the Office Action). Applicant submits that FET MN13 cannot be both part of the gain stage and part of the impedance divider.

With respect to the §103 rejection, Neither Jaussi nor Narendra disclose or suggest an impedance divider directly coupled to a supply voltage source of a current mirror circuit.

In particular, FIG. 2 of Jaussi is an example of a variable resistor used for the variable resistor 120 of FIGS. 1A and 1B. The Examiner has suggested that the variable resistor 200 may be used as an impedance divider (see pages 3 and 4 of the Office Action). Even if the variable resistor 200 is used in FIGS. 1A and 1B for the variable resistor, the variable resistor 120 is not connected to the supply voltage of the current mirror 102.

Likewise in Narendra, the Examiner has indicated that the variable resistor 200 may be used as an impedance divider in FIG. 1. Even if the variable resistor 200 is used in FIG. 1 for the variable resistor, the variable resistor 120 is not connected to the supply voltage of the current mirror 102.

Based on the foregoing reasons, Applicant submits that claim 1 is allowable.

With regards to amended claim 6, Applicant submits that claim 6 is allowable for at least the same reasons as claim 1.

With regards to the means claim 9, Applicant respectfully submit that claim 9 is a means claim under 35 U.S.C. §112 and allowable because none of the prior art cited by the Examiner has disclosed the structure indicated in the specification (see MPEP 2181 and In re Donaldson Co., 16 F.3d 1189).

Applicant respectfully requests withdrawal of the art rejections.

Applicant submits that all dependent claims now depend on allowable independent claims.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Applicant submits that the entire application is now in condition for allowance. Such action is respectfully requested at the Examiner's earliest convenience.

All correspondence should be directed to the address below. Applicant's attorney can be reached by telephone at (781) 401-9988 ext. 23.

No fee is believed to be due for this Response; however, if any fees are due, please apply such fees to Deposit Account No. 50-0845 referencing Attorney Docket: TER-024PUS.

Respectfully submitted,

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